AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)

10. (Withdrawn) A flip-flop circuit comprising:

(a) a first branch comprising a P type transistor and an N type transistor connected in series, the drain of said P type transistor being connected to a first branch drain node and the source of said N type transistor being connected to a low potential;

(b) a second branch comprising a P type transistor and an N type transistor connected in series, the drain of said P type transistor being connected to a second branch drain node and the source of said N type transistor being connected to a low potential, said drain node being common with said drain node of said first branch

(c) a shared transistor having its drain connected to said drain nodes of said first and second branches; and

(d) a pulse generator connected to the gate of said shared transistor.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (New) A flip-flop circuit comprising:

(a) a first branch having two transistors in series and a first branch source node, said first branch comprising a P-type transistor and an N-type transistor connected in series, the source of said N-type transistor being connected to said first branch source node and the drain of said P-type transistor being connected to a high potential;

(b) a second branch having two transistors in series and a second branch source node, said second branch comprising a P-type transistor and an N-type transistor connected in series, the source of said N-type transistor being connected to said second branch source node and the drain of said P-type transistor being connected to said high potential, said second branch source node being common with said first branch source node;

(c) a shared transistor having its source connected to said first branch source node and said second branch source node;

(d) a pulse generator connected to the gate of said shared transistor; and

(e) wherein the source of said first branch P-type transistor is connected to a first branch latch and the source of said second branch P-type transistor is connected to a second branch latch.

17. (New) The flip-flop circuit of claim 16 wherein said latches include means for retaining the value in said latches even when disconnected from the circuit.

18. (New) The flip-flop circuit of claim 17 wherein said value retaining means includes back to back inverters, one inverter being selected to be weaker than the other inverter.

19. (New) A flip-flop circuit comprising:

(a) a first branch having two transistors in series and a source node;

(b) a second branch having two transistors in series and a source node, said source node being common with said source node of said first branch;

(c) a shared transistor having its source connected to said source nodes of said first and second branches; and

(d) a pulse generator connected to the gate of said shared transistor; said pulse generator comprising:

(i) an inverter chain having:

(1) an input node for receiving a clock signal; and

(2) an output;

(ii) a NAND having an output and two inputs, one of said NAND inputs connected to said inverter chain input node and the other of said NAND inputs connected to said output of said inverter chain; and

(iii) an inverter having an input and an output, said inverter input connected to said output of said NAND and said inverter output connected to the gate of said shared transistor.

20. (New) The flip-flop circuit of claim 16 further comprising:

(a) a data signal input connected to the gates of said first branch P type transistor and said first branch N type transistor; and

(b) a data inverter having an input and an output, said data inverter input connected to said data signal input and said data inverter output connected to the gate of said second branch N type transistor.

21. (New) The flip-flop circuit of claim 16 further comprising:

(a) a data signal input connected to the gates of said first branch P type transistor and said first branch N type transistor; and

(b) a data inverter having an input and an output, said data inverter input connected to said data signal input and said data inverter output connected to the gate of said second branch N type transistor.

22. (New) A static explicit pulsed flip-flop circuit comprising:

(a) a first branch having three transistors in series, one of said first branch transistors being a clocked transistor and the other two transistors being non-clocked transistors having their gates connected to a data input;

(b) a second branch having three transistors in series, one of said second branch transistors being a clocked transistor and the other two transistors being non-clocked transistors having their gates connected to a node between said first branch non-clocked transistors;

(c) a pulse generator connected to the gates of said clocked transistors in said first and second branches; and

(d) wherein said gates of said second branch non-clocked transistors are connected to a first branch latch and a second branch latch is connected between said second branch non-clocked transistors.

23. (New) The flip-flop circuit of claim 22 wherein said latches include means for retaining the value in said latches even when disconnected from the circuit.

24. (New) The flip-flop circuit of claim 23 wherein said value retaining means includes back to back inverters, one inverter being selected to be weaker than the other inverter.